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EXAMINER	
JOHNSON, BRIAN P	

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2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,338	MCDONALD, THOMAS C.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21-23,35-38 and 40* is/are rejected.

7)☐ Claim(s) *20,24 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-40 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS, on August 19th, 2003. The papers filed have been placed on record.

Claim Objections

2. Claims 4, 15 and 22 are objected to because of the following informalities:

Regarding claim 4, "the internal call/return stack" lacks antecedent basis.

Regarding claims 15 and 22, the language appears to be unclear. See the rejections of claims 15 and 22 for more information.

Appropriate action is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 40 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The computer-readable medium is listed in the specification to include a transmission medium which is not tangible and, therefore, is considered to be non-statutory subject matter.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371 (c) of this title before the invention thereof by the applicant for patent.

5. Claims 30 and 33-38 are rejected under 35 U.S.C. 102(e) as being anticipated by D'Sa (U.S. Patent No. 6,374,350)..

6. Regarding claim 30, D'Sa discloses a pipelined microprocessor, comprising: a call/return stack (CRS); first (fig 1a reference 910) and second pipeline stages (fig 1a reference 920), for generating a true value on first and second signals, respectively, in response to detection of a misprediction of a branch instruction present in said first and second pipeline stage (col 14 lines 25-26 and col 8 lines 3-11), respectively, wherein said first stage is above said second stage in the pipeline (fig 1a); an apparatus, coupled to receive said first and second signals, for maintaining first information related to call or return instructions present in stages of the pipeline above said first stage (fig 1a reference 911), and for maintaining second information related to call or return instructions present in stages of the pipeline between said first and second stages (fig 1a reference 921), wherein said apparatus is configured to selectively correct said CRS using said first information if said first signal is true (col 4 lines 44-46), or said first and second information if said second signal is true (col 4 line 65 to col 5 line 4).

Note that the signals that suggest a branch misprediction, as described in col 8 lines 3-11 would cause a correction in the speculative stacks.

7. Regarding claim 33, D'Sa discloses the microprocessor of claim 30, further comprising: a third signal, received by said apparatus, for indicating detection of an exception generated by an instruction present in said second pipeline stage; wherein said apparatus corrects said CRS using said first and second information if said third signal is true (col 4 line 65 to col 5 line 4 col 50 lines 53 to 54).

8. Regarding claim 34, D'Sa discloses a method for maintaining consistency between a call/return stack (CRS) in a pipelined microprocessor and a memory coupled thereto, the method comprising: receiving requests to update the CRS in response to a presence of call or return instructions (col 4 line 9 and and col 4 lines 54 to 65); storing correction information into a first buffer, in response to said receiving (col 4 lines 54-58 and col 5 lines 10-11); detecting a condition in which one of the call or return instructions has proceeded past a first stage of the microprocessor pipeline configured to detect an invalidating event (col 5 lines 34-44), after said storing (col 4 line 65 to col 5 line 4); and moving a portion of the correction information from the first buffer to a second buffer, in response to said detecting (col 4 line 65 to col 5 line 4).

9. Regarding claim 35, D'Sa discloses the method of claim 34, wherein said invalidating event comprises a branch instruction misprediction (col 14 lines 25-26).

10. Regarding claim 36, D'Sa discloses the method of claim 34, further comprising: correcting the CRS with the correction information stored in the first buffer if the first stage detects the invalidating event (col 5 lines 34-44).

Note that choosing information in the real stack (first buffer) rather than the speculative stack is considered to be correcting the CRS. Note the use of valid bits in fig 2b.

11. Regarding claim 37, D'Sa discloses the method of claim 36, further comprising: correcting the CRS with the correction information stored in the first and second buffer if a second stage of the microprocessor pipeline detects a second invalidating event (col 5 lines 34-44), wherein the second stage is below the first stage (fig 1a).

12. Regarding claim 38, D'Sa discloses the method of claim 37, wherein said invalidating event comprises a branch instruction misprediction (col 8 lines 3-11). .

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-19, 21-23 and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable by D'Sa (U.S. Patent No. 6,374,350) in view of Computer Architecture and Design (herein Hennessy).

15. Regarding claim 1, D'Sa discloses an apparatus for correcting a call/return stack in a pipelined microprocessor (col 4 lines 44-47), the apparatus comprising: a first stack (fig 1a reference 911), comprising a first plurality of entries for storing correction information related to call or return instructions present in a first plurality of stages of the microprocessor pipeline (col 4 lines 54-58 and col 5 lines 10-11);

Note that fig 1a shows that the stack represents only a portion of the pipeline stages. Also note, on col 5 lines 10-11 that a real return stack buffer with "correction information" may be maintained be "one or more pipeline units", even though the real stack buffer is only pictured in the third pipelien stage in figure 1a.

A second stack (fig 1a reference 921), coupled to said first stack (fig 1a),

Note that the connection is indirect through the pipeline units, but still exists.

Comprising a second plurality of entries for storing correction information related to call or return instructions present in a second plurality of stages of the microprocessor pipeline (col 4 lines 54-58 and col 5 lines 10-11); and control logic, coupled to said first and second stacks (fig 1a), for receiving a control signal indicating a call or return instruction is passing from said first plurality of stages to said second plurality of stages (see below),

Note that for this claim, and others disclosing a "control signal", if the reference contains a means for completing the claimed limitation, the control signal must exist to trigger the action.

D'Sa fails to disclose control that logic moves said correction information associated with said call or return instruction from said first stack to said second stack in response to said control signal.

Hennessy discloses instructions that propagate down the pipeline and have data associated to those instructions follow down the pipeline, getting moved from register to register (page 469).

Allowing the data associated to an instruction to have a spatial relationship with its associated data can reduce the complexity of a processing system. D'Sa would be motivated to have the data associated with the instructions follow the instruction as it is moved down the pipeline in order to keep the data appropriately organized. Additionally, depending on the layout of the processor, this technique can reduce latency by keeping data in a close proximity to the instruction, in order to increase clock frequency and performance.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the system of D'Sa have the return address data follow the instruction as it propagates down the pipeline (as in Hennessy). This combination would cause the return addresses to be popped and pushed from a particular stack into the subsequent stack (which already exist win D'Sa fig 1a references 911, 921 and 931) as the instruction is propragated.

16. Regarding claim 2, D'Sa/Hennessy discloses the apparatus of claim 1, wherein said control logic moving said correction information associated with said call or return instruction from said first stack to said second stack comprises said control logic removing said correction information from a bottom valid one of said first plurality of entries in said first stack (col 4 line 65 to col 5 line 4)

Note in particular the term "popped" on col 5 line 2

And pushing said removed correction information onto said second stack (col 5 lines 2-4).

17. Regarding claim 3, D'Sa/Hennessy discloses the apparatus of claim 2, wherein said control logic removing said correction information from said bottom valid one of said first plurality of entries in said first stack comprises invalidating said bottom valid one of said first plurality of entries in said first stack (col 11 lines 42-44).

Note that, clearly, as the stack is popped, the entry is invalidated.

18. Regarding claim 4, D'Sa/Hennessy discloses the apparatus of claim 1, wherein if said related call or return instruction is a call instruction, said correction information comprises a command to pop a return address off the internal call/return stack (col 4 line 65 to col 5 line 4).

Note that, as combined with Hennessy, for the return addresses to be moved down the pipeline while following the instructions, the addresses must be popped off the first stack's pipeline before they can be pushed onto the subsequent stack's pipeline.

19. Regarding claim 5, D'Sa/Hennessy discloses the apparatus of claim 1, further comprising: a third stack (col 5 lines 10-11), coupled to said control logic, comprising a third plurality of entries for storing return addresses related to call instructions present in said first or second plurality of pipeline stages (col 5 lines 10-28 or col 3 line 62 to col 4 line 6).

Note that there are two ways that the third stack is anticipated. 1) the "real" stack addresses are considered to be related to the call instructions present in said first or second plurality of pipeline stages and 2) D'Sa/Hennessy discloses that there are potentially more than two pipeline units (each with a separate stack). Another stack (associated with a pipeline unit before the first and second stacks) is considered to be the "third stack" as well.

20. Regarding claim 6, D'Sa/Hennessy discloses the apparatus of claim 5, wherein if said related call or return instruction is a return instruction, said correction information comprises a command to pop a return address off said third stack and push said return address onto the internal call/return stack (col 3 line 62 to col 4 line 6).

Note that, as combined with Hennessy, the addresses must follow the instructions to their respective stack registers. If, for instance, there was a 4th stack,

note col 4 lines 52-54, the third stack will give an address to the 4th stack, which is included in the "internal call return stack", the internal call/return stack considered to be all stacks associated to call/return addresses.

21. Regarding claim 7, D'Sa/Hennessy discloses the apparatus of claim 1, further comprising: a plurality of valid bits (fig 2a reference 210), coupled to said first stack (col 8 lines 43-51), for specifying whether corresponding ones of said first plurality of entries are valid (col 8 lines 52-55).

22. Regarding claim 8, D'Sa/Hennessy discloses the apparatus of claim 1, further comprising: a plurality of valid bits (fig 2a reference 210), coupled to said second stack (col 8 lines 43-51), for specifying whether corresponding ones of said second plurality of entries are valid (col 8 lines 52-55).

23. Regarding claim 9, D'Sa/Hennessy discloses the apparatus of claim 1, wherein said control signal indicates said call or return instruction has reached a bottom stage of said first plurality of pipeline stages (col 4 line 65 to col 5 line 4).

Note that for the stack address to propagate down the pipeline, a signal must indicate when the instruction has reached the bottom stage for the stacks to be updated correctly.

24. Regarding claim 10, D'Sa/Hennessy discloses the apparatus of claim 9, wherein said control signal indicates said bottom stage of said first plurality of pipeline stages is not stalled (col 9 lines 33-36).

Note that if a stall can occur, a control signal must exist to indicate the stall. So, clearly, because computers run on binary logic, this signal must also indicate that there is no stall.

25. Regarding claim 11, D'Sa/Hennessy discloses the apparatus of claim 10, wherein said control signal indicates a branch instruction preceding said call or return instruction has not been detected as mispredicted by the microprocessor (col 8 lines 3-11).

Note that the misprediction recovery would be one possibility of a stall. The signal, indicating that there is no stall, must also indicate that there is no branch misprediction, because said prediction would cause a stall.

26. Regarding claim 12, D'Sa/Hennessy discloses the apparatus of claim 1, further comprising: a second control signal, received by said control logic, for indicating said call or return instructions present in said first plurality of pipeline stages were speculatively incorrectly executed (col 9 lines 37-45).

27. Regarding claim 13, D'Sa/Hennessy discloses the apparatus of claim 12, wherein said second control signal indicates a branch instruction preceding said call or

return instructions present in said first plurality of pipeline stages was mispredicted by the microprocessor (col 8 lines 3-11).

Note that the misprediction recovery would be one possibility of a stall. The signal, indicating that there is no stall, must also indicate that there is no branch misprediction, because said prediction would cause a stall.

28. Regarding claim 14, D'Sa/Hennessy discloses the apparatus of claim 12, wherein said second control signal indicates one of said call or return instructions present in said first plurality of pipeline stages was mispredicted by the microprocessor (col 9 lines 37-45).

29. Regarding claim 15, D'Sa/Hennessy discloses the apparatus of claim 12, wherein said second control signal is generated by a bottom stage of said first plurality of pipeline stages (col 9 lines 37-45 and fig 1a reference 911).

Note that saying that a control signal is generated by a particular stage in a pipeline does not appear to have any real meaning. Signals are created by separate modules that may or may not be considered to be part of a pipeline depending how how the invention is conceptually viewed, but makes no apparent difference to the invention itself. Perhaps this claim is intended to indicate that the control signal is generated during a clock cycle in which the instructions that caused the signal generation are being processed by the bottom stages of the pipeline. If this is the case, the misprediction signal will clearly be raised immediately when a misprediction is detected.

So, if the detection is related to an instruction in the first pipeline unit or fig 1 reference 910, that is when the signal will be raised.

30. Regarding claim 16, D'Sa/Hennessy discloses the apparatus of claim 12, wherein said control logic corrects the call/return stack using said correction information stored in said first plurality of entries of said first stack (col 5 lines 34-44), in response to said second control signal.

31. Regarding claim 17, D'Sa/Hennessy discloses the apparatus of claim 16, wherein for each valid one of said first plurality of entries, said control logic pops a top said valid one of said first plurality of entries from said first stack, and corrects the call/return stack based on said correction information stored therein (col 5 lines 34-44).

32. Regarding claim 18, D'Sa/Hennessy discloses the apparatus of claim 16, further comprising: a third control signal, received by said control logic, for indicating said call or return instructions present in said first and second plurality of pipeline stages were speculatively incorrectly executed (col 9 lines 33-45).

33. Regarding claim 19, D'Sa/Hennessy discloses the apparatus of claim 18, wherein said third control signal indicates a branch instruction preceding said call or return instructions present in said first and second plurality of pipeline stages was mispredicted by the microprocessor (col 8 lines 3-11).

34. Regarding claim 21, D'Sa/Hennessy discloses the apparatus of claim 18, wherein said third control signal indicates one of said call or return instructions present in said first and second plurality of pipeline stages was mispredicted by the microprocessor (col 9 lines 33-45).

35. Regarding claim 22, D'Sa/Hennessy discloses the apparatus of claim 18, wherein said third control signal is generated by a bottom stage of said second plurality of pipeline stages (col 9 lines 37-45 and fig 1a reference 921).

See claim 15

36. Regarding claim 23, D'Sa/Hennessy discloses the apparatus of claim 18, wherein said control logic corrects the call/return stack using said correction information stored in said first and second plurality of entries of said first and second stacks, in response to said third control signal (col 5 lines 34-44).

Note that, clearly, the branch misprediction would cause a mispredicted address to be recovered.

37. Regarding claim 25, D'Sa/Hennessy discloses the apparatus of claim 1, further comprising: a second signal, received by said control logic, for indicating one of said call or return instructions present in said second plurality of stages of the microprocessor

pipeline is no longer speculative (col 14 lines 10-29), wherein said control logic updates said second stack in response to said second signal (col 14 lines 25-26).

Note that when a return address is considered to be invalid, it is no longer speculative.

38. Regarding claim 26, D'Sa/Hennessy discloses the apparatus of claim 25, wherein said control logic updating said second stack in response to said second signal comprises invalidating one of said second plurality of entries storing said correction information for said no longer speculative one of said call or return instructions (col 11 lines 42-44).

Note that the entry is marked invalid, indicating that the entry is no longer speculative.

39. Regarding claim 27, D'Sa/Hennessy discloses the apparatus of claim 26, wherein said invalidating one of said second plurality of entries storing said correction information for said no longer speculative one of said call or return instructions comprises invalidating a bottom valid one of said second plurality of entries (col 11 lines 42-44).

40. Regarding claim 28, D'Sa/Hennessy discloses the apparatus of claim 1, further comprising: a second signal, received by said control logic, for requesting the call/return stack be updated in response to the presence of one of said call or return instructions in

said first plurality of pipeline stages, wherein said control logic stores correction information related to said one of said call or return instructions into said first stack in response to said second signal (col 11 lines 21-32).

41. Regarding claim 29, D'Sa/Hennessy discloses the apparatus of claim 28, wherein said control logic storing said correction information related to said one of said call or return instructions into said first stack comprises said control logic pushing said correction information onto said first stack (col 5 lines 34-44 and col 5 lines 29-33).

Note that the first stack, in some embodiments, includes both the real and speculative register.

42. Regarding claim 31, D'Sa/Hennessy (as combined in claim 1) discloses the microprocessor of claim 30, further comprising: a third signal, received by said apparatus, for indicating one of said call or return instructions has arrived in said first stage; wherein said apparatus transfers to said second information a portion of said first information related to said one of said call or return instructions, in response to said third signal.

Note that it is presumed that this claim is referring to propagating return address information along with the instructions. See claim 1.

43. Regarding claim 32, D'Sa/Hennessy (as combined in claim 1) discloses the microprocessor of claim 30, further comprising: a third signal, received by said apparatus, for indicating one of said call or return instructions has arrived in said second stage wherein said apparatus removes from said second information a portion of said second information related to said one of said call or return instructions arrived in said second stage, in response to said third signal.

Note that, similar to claim 31, this claim is presumed to refer to the propagation of return addresses and is anticipated with the combination of D'Sa/Hennessy in claim 1.

44. Regarding claim 40, D'Sa discloses a computer data signal embodied in a transmission medium (col 4 lines 9-10), comprising: computer-readable program code for providing an apparatus for correcting a call/return stack in a pipelined microprocessor (col 5 lines 34-44), said program code comprising: first program code for providing a first stack (fig 1a reference 911), comprising a first plurality of entries for storing correction information related to call or return instructions present in a first plurality of stages of the microprocessor pipeline (col 5 lines 10-11 and fig 2b reference 123); second program code for providing a second stack (fig 1a reference 921), coupled to said first stack (fig 1a),

Note that the arrows in figure 1a signify coupling wires.

Comprising a second plurality of entries for storing correction information related to call or return instructions present in a second plurality of stages of the microprocessor

pipeline (col 5 lines 10-11 and fig 2b reference 123); and third program code for providing control logic,

Note that the claimed "control logic" must exist of the effect of the control logic is disclosed in the reference. There must be some hardware controlling this effect, which is considered to be the control logic.

Similarly to claim 1, D'Sa fails to disclose moving the return addresses to a pipeline stage's appropriate stack when the instruction propagates down the pipeline. See claim 1 for combination and motivation with Hennessy.

Allowable Subject Matter

45. Claims 20, 24 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 20, prior art fails to disclose limitations on which claim 20 is dependent in addition to an exception generated for the branch misprediction.

Regarding claim 24, prior art fails to disclose limitations on which claim 24 is dependent in addition to the particular correction method described.

Regarding claim 39, prior art fails to disclose limitations on which claim 39 is dependent in addition to an exception generated for the branch misprediction.

Conclusion

46. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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